WHAT IS CLAIMED IS

1. A surge suppression circuit comprising:

first and second transistors which are arranged as a complementary Darlington pair.

2. A surge suppression circuit as set forth in claim 1, further comprising:

a resistor connected between the emitter of the first transistor and the base of the second transistor; and

a Zener diode connected between the base of the second transistor and ground.

3. A surge suppression circuit as set forth in claim 1, wherein the first transistor is a PNP type transistor and wherein the second transistor is a NPN type transistor

4. A surge suppression circuit as set forth in claim 1, wherein the collector of the second transistor is connected to the base of the first transistor.

5. A surge suppression circuit as set forth in claim 2, further comprising a diodes circuited with the emitter of the first transistor.

6. A surge suppression circuit as set forth in claim 2, wherein the resistor is connected to a junction between the diode and the emitter of the first transistor.

7. A surge suppression circuit as set forth in claim 2, further comprising a capacitor connected between ground and the base of the second transistor.

8. A method of surge suppression comprising interposing a complementary Darlington pair between an input and output.

9. A method as set forth in claim 8, wherein the complementary Darlington pair is configured by:

using a PNP transistor as the first transistor;

using a NPN transistor as the second transistor; and

connecting the base of the first transistor to the collector of the second transistor

10. A method as set forth in claim 9, further comprising:
arranging a resistor between the input and a base of the second transistor; and
connecting the base of the second transistor to ground via a Zener diode.